ABOLFAZL AZAD

ELECTRICAL ENGINEERING B.Sc. CANDIDATE | RTL DESIGN | HARDWARE ACCELERATION

Tehran, Iran • abolfazlazad@ut.ac.ir • Website • LinkedIn • GitHub

PROFESSIONAL PROFILE

Electrical Engineering B.Sc. candidate at the University of Tehran focused on digital systems, RTL design, and computer architecture. Project experience includes SystemVerilog-based matrix-multiplication accelerator design and verification, SystemC-based FIR accelerator integration, and open-source RISC-V SoC verification. Supervised research spans low-power RTL optimization, hardware-aware weight quantization, and NeuroSim-based memristor/CIM characterization. Seeking research experience in energy-efficient digital design, hardware accelerators, RISC-V systems, and AI hardware.

EDUCATION

University of Tehran | Tehran, Iran 2023–2028 (expected)

B.Sc. candidate in Electrical Engineering. Focus: Digital Systems.

Cumulative GPA: 17.11/20

Minor candidate in Computer Engineering.

RESEARCH INTERESTS

Low-power RTL and switching-activity reduction; hardware accelerators and datapath/control design; computer architecture and RISC-V; hardware/software co-design; compute-in-memory (CIM); memristor-based neural networks and low-bit weight quantization.

RESEARCH EXPERIENCE

Matrix-Multiplication Hardware Accelerator (iMPAC)

University of Tehran | Supervised by Prof. Zainalabedin Navabi

- **RTL implementation and verification.** Contributed across processing-element datapaths, control logic, and I/O integration; used a SystemVerilog testbench and simulation flow to validate functionality.

Low-Power RTL Optimization for iMPAC

University of Tehran | Supervised by Prof. Zainalabedin Navabi

- **Switching-activity reduction.** Investigating operation-aware operand isolation in the add/sub datapath and pre-multiplexer isolation variants to reduce unnecessary switching. Functional simulation and synthesis/timing comparisons are ongoing; quantitative power and area gains remain under evaluation.

Weight Quantization for Memristor-Based Neural Networks

University of Tehran | Supervised by Dr. Shaghayegh Vahdat

- **Hardware-aware quantization.** Investigating weight-mapping and clustering-based strategies to retain model accuracy at a fixed 3-bit representation. Planned evaluation compares quantization baselines and considers fine-tuning and quantization-aware training (QAT); this is ongoing work, not a published result.

NeuroSim-Based Compute-in-Memory Inference Characterization

University of Tehran | Supervised by Dr. Shaghayegh Vahdat

- **RRAM-oriented simulation.** Set up an inference simulation path with a 128 × 128 subarray, 5-bit ADC, and VGG8/CIFAR-10 baseline. Exploring how circuit assumptions and quantization choices affect estimated area, energy, and latency; results are simulation estimates, not silicon measurements.

OPEN-SOURCE CONTRIBUTIONS

- **NEORV32 — GPIO input loopback verification.** Added a repeatable input pattern and masked input checks to processor_check; included in upstream release notes. PR #1643
- **NEORV32 — Floating-point test correction.** Fixed unreachable special values and signaling-NaN handling in the floating_point_test software test. PR #1644

INDUSTRY EXPERIENCE

Pars Khodro | Electrical Engineering Intern Jul–Sep 2026

Digital Motor Control & Embedded Systems | Iran

- **Traction-inverter analysis.** Examined TI TIDM-02017 and digital motor-control topics including C2000/CLA, ADC, ePWM, FOC, SVPWM, and MTPA.
- **Digital control chain.** Studied the path from sensing and signal processing through PWM generation and gate-driver control.

TEACHING EXPERIENCE

University of Tehran | Tehran, Iran

Laboratory Teaching Assistant — Digital Systems I: Oct 2026–Present; supervised by Dr. Navabi (Fall 2026).

Teaching Assistant — Computer Architecture (Digital Systems II): Sep 2026; supervised by Dr. Saeed Safari (Fall 2026).

Teaching Assistant — Signals and Systems: Jan 2026–Present; supervised by Dr. Saeed Akhavan (Spring and Fall 2026).

Teaching Assistant — Digital Systems I: Jan–Aug 2026; supervised by Dr. Navabi (Spring 2026).

TECHNICAL SKILLS

HDL & RTL: Verilog, SystemVerilog, VHDL; RTL design; FSMs; datapath/control design; testbench-based verification.

Simulation & FPGA: QuestaSim/ModelSim, Quartus, Xilinx Vivado, GHDL, Verilator; simulation/debugging and FPGA-oriented workflows.

Synthesis & physical design: Synopsys Design Compiler, Cadence Innovus; RTL synthesis and physical-design tools.

Systems & architecture: SystemC, C/C++, RISC-V/NEORV32, memory-mapped I/O, interrupts, DMA, and system-bus integration.

Research & software: Python, PyTorch for research prototyping, NeuroSim; memristor/CIM modelling and quantization research in progress.

Development environment: Git/GitHub, Linux/WSL, command-line build and simulation workflows.

LANGUAGES

Persian: Native | **English:** Fluent

SELECTED COURSEWORK

Electrical Engineering: Digital Electronics; Digital Systems I; Computer Architecture; Object-Oriented Programming; ASIC Design; Electronic System-Level (ESL) Design; FPGA-Based Embedded Systems.

Computer Engineering minor: Advanced Programming; Data Structures and Algorithms; Operating Systems.